



## Open Archive Toulouse Archive Ouverte (OATAO)

OATAO is an open access repository that collects the work of some Toulouse researchers and makes it freely available over the web where possible.

This is an author's version published in: <https://oatao.univ-toulouse.fr/21810>

**Official URL :** <http://doi.org/10.1109/TED.2016.2516045>

### To cite this version :

Marcelot, Olivier and Molina, Romain and Bouhier, Matthieu and Magnan, Pierre Design Impact on Charge Transfer Inefficiency of Surface CCD on CMOS Devices: TCAD and Characterization Study. (2016) IEEE Transactions on Electron Devices, 63 (3). 1099-1104. ISSN 0018-9383

Any correspondence concerning this service should be sent to the repository administrator:

[tech-oatao@listes-diff.inp-toulouse.fr](mailto:tech-oatao@listes-diff.inp-toulouse.fr)

# Design Impact on Charge Transfer Inefficiency of Surface CCD on CMOS Devices: TCAD and Characterization Study.

O. Marcelot, R. Molina, M. Bouhier, P. Magnan

**Abstract**—This work presents a study of design optimization of CCD on CMOS devices, in order to minimize the Charge Transfer Inefficiency (CTI). To achieve this goal, 3D Technology Computer Aided Design (TCAD) simulations with a trap model at silicon–oxide interface were conducted, and measurements on two test chips manufactured on two different foundries were performed. TCAD simulations predict trends in agreement with measurements, but trap models at STI and gate oxides should be adapted accordingly to the technology used. Some design variations show results depending on the technology chosen, and the best CTI reduction is obtained with an increase of Pwell inclusion over STI edges.

**Index Terms**— Charge coupled devices, charge transfer, charge, transfer inefficiency, CMOS image sensors (CIS), deep submicrometer process, trapped charge.

## I. INTRODUCTION

Nowaday, CMOS image sensors are widely used for commercial and scientific applications, because they have made huge progress and they have now very competitive performances [1][2]. In addition, they have the possibility to integrate CMOS functions and offer a high integration for a lower cost. However, real CCD devices are still dominating in specific field like TDI imaging [3]. Indeed, in contrary to CCD process, CMOS imaging submicronic processes do not provide CCD optimizations like for example high oxide quality or poly-silicon overlapping. As a consequence, dark currents are generally more important and the charge transfer inefficiency (CTI) is higher due to the presence of poly-silicon gap between gates. However, thanks to the latest advances in manufacturing process, it becomes possible to realize CCD devices on CMOS technology. Consequently, a very strong need for the integration of CCD devices on CMOS technology is emerging in order to combine the advantages of CMOS integration, photodiodes and pinned photodiodes, and charge transfer along long distances with high performance.

As written before, CMOS imaging processes do not offer gates overlapping option and a gap between gates remains and leads to a weak electric field which can delay or even lose

charge during transfer [4]. This gap is forced by design rules and is usually higher than 200 nm. The other main weakness is the lower surface oxide quality of the CMOS processes responsible of higher dark current. One alternative exists and is the use of a Buried channel implant (BCCD) [5]. This additional implant creates a buried potential well, and electrons are thus carried away from the surface, which improves the charge transfer and decreases the dark current. However this special implant is usually not proposed by CMOS image sensor foundries, and we choose not to use it in order to keep a conventional process. Performances of CCD on CMOS devices are thus inferior to real CCD devices, for example CTI in CCD on CMOS achieves some  $10^{-3}$  [6]-[7]-[8] while CTI is kept below  $10^{-5}$  in real CCD [9]-[10].

Therefore, it is of primary interest to develop new strategies with the goal to improve CCD on CMOS performances. As we want to keep the lower cost and the accessibility of conventional CMOS image sensor fab, process modifications should not be developed. Thus, the remaining possibility is to develop solutions based on design adjustments.

In this paper, we propose firstly to explore some design modifications with 3D TCAD simulations, and then secondly to measure dedicated test vehicles containing the selected design variations.

## II. 3D TCAD INVESTIGATION

3D TCAD simulations were conducted with the Synopsys Sentaurus software. The structure was created using Sentaurus Device Editor (SDE) and analytical profiles for the Pwell, source and drain implantations, and then imported in Sdevice for electrical simulations. All simulated structures have the same elements: four gates, one drain, and one ground contact (Fig. 1). The poly-silicon thickness and the poly-silicon gap are fixed respectively at 200 nm and at 100 nm.

Gates are polarized at conventional CMOS values, i.e.  $V_{low} = 0$  V and  $V_{max} = 3.3$  V. Before injecting electrons the TCAD structure is reseted through the N-plus drain. Following this operation, electrons are injected under the gate “1” using an optical illumination. Then the charge packet is moved gate by gate until gate “3”, keeping the gate “4” at  $V_{low}$ . The transient signal applied on the gates is characterized by 100 ns pulse widths with 10 ns ramps edges.

Due to the presence of surface states, potential barrier between gates due to the poly-gap and silicon bulk defects,

electrons can be trapped and eventually re-emitted when the charge packed is moved to the following gates. This singularity is at the origin of CTI, which gives the ratio of electrons missed or lost after one transfer. Some of these electrons are transported in the following transfer phases, and they are called “deferred electrons”. The other ones are lost.

With the aim of getting closer to experimental results, a trap model was introduced during the charge transfer between gates. Indeed, without this defect model, the CTI would be ideally null [11]. In Sdevice, acceptors are specified at all silicon – oxide interfaces, with a concentration of  $5 \times 10^9$  traps.cm<sup>-2</sup> and a capture cross sections of  $1 \times 10^{-15}$  cm<sup>2</sup>.

The CTI is estimated by comparing injected electrons under gate “1” ( $n_{e-inj.}$ ) with transferred electrons ( $n_{e-transf.}$ ) under gate “3”:

$$CTI = \frac{n_{e-inj} - n_{e-transf}}{n_{e-inj} \times 2} \quad (1)$$

where 2 is the transfer number. The CTI extracted from TCAD simulation is therefore based on deferred and lost charge.

The TCAD mesh was chosen to give the best compromise between calculation time and precision. CCD structure meshes have an average of 200000 elements, implying a simulation time between 10 h and 20 h (Fig. 1).

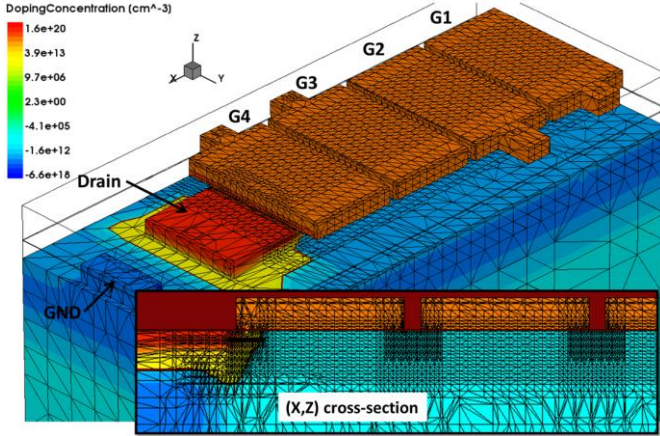


Fig. 1. 3D TCAD doping concentration of the reference CCD structure and visualization of the mesh, without oxide regions. A (X,Z) cross-section illustrates the CCD channel mesh precision.

Initially, a reference design (“REF”) is defined with a conventional gate conformation: poly-silicon rectangular gates larger than the diffusion area (Fig.1). With the aim to avoid any dark current generation due to a contact of the depleted region with the Silicon Trench Isolation (STI), STI edges are enclosed within 100 nm of P-well. Gate area on diffusion region without Pwell is  $1 \mu\text{m} \times 1 \mu\text{m}$ .

#### A. Gate conformation

The gate shape modification over the CCD channel is the first investigation presented. Two designs are proposed with a “V” shape (Fig. 2). The purpose is to improve the transfer in

one direction. Indeed, under the narrowest part of the gate the potential in the channel as well as the well capacity are expected to be lower due to narrow channel effect. Charge should tend to migrate to the widest part of the gate, which improves the transfer. However this modification has a drawback, as the structure can only transfer charge in only one direction. The design called “form 1” has a wide section on the left part of the gate to optimize the electron transfer from the previous gate. Then, a “V” shape should help the electron transfer to the right side part of the gate. The design called “form 2” has a thin section on the left part of the gate and is based on a “V” shape.

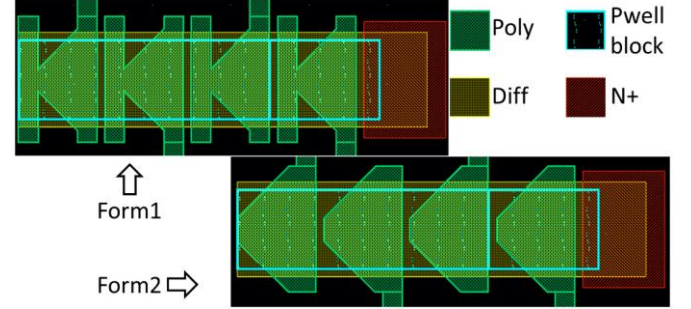


Fig. 2. Design view of the two modified structures with a “V” gate conformation.

The Fig. 3 is showing the TCAD CTI results for the reference and the two modified designs.

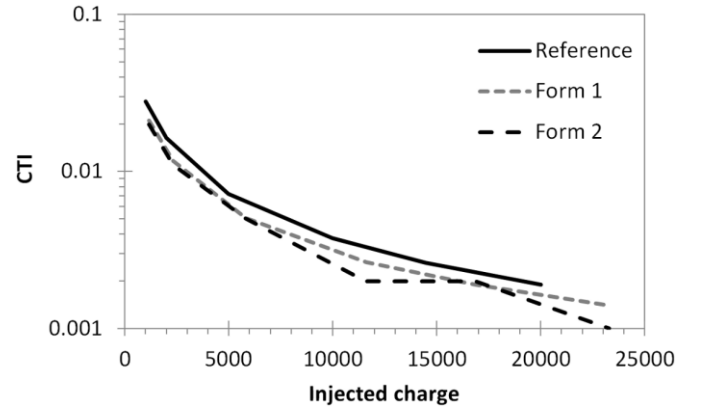


Fig. 3. 3D TCAD simulation of Charge Transfer Inefficiency vs injected charge of three different gate designs.

As it can be seen on the Fig. 3, the gate conformation modifications reduce the CTI up to 45%. The “form 2” which only has a “V” shape gives the best result. In the “form 1” the wide left part followed by the “V” shape is not the best option to optimize the electron transfer. Indeed, electrons stored under the left wide part of the gate hardly go through funnel gate which has an unfavorable potential distribution. From these results, it can be seen that a thin section on the left part of the gate (like in “form 2”) does not trouble the charge transfer from a gate with a wide section. According to these observations, only the “form 2” design is chosen to be implemented in the test chip.

### B. Gates avoided on STI area

The idea of this modification is to entirely remove STI edges from the CCD channel with the goal to minimize charge trapping at STI edges. Indeed, generally STI edges introduce a higher number of interface states than surface oxide [12], depending on the foundry used. To do so, the poly-silicon gates were only drawn on the diffusion layer (Fig. 4), and the poly-silicon contacts are drawn on the diffusion area. The expected result is a reduction of charge trapping and a reduction of CTI.

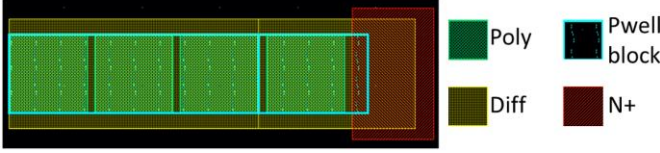


Fig. 4. Design view of the CCD structure with gates only on diffusion layer. STI edges are not in contact with the CCD channel.

The Fig. 5 shows the TCAD simulation of CTI with this design modification. A small decrease of CTI is visible at all injection levels. Two cross-sections extracted from the simulated CCD structure are grouped in the Fig. 6. These cross-sections perpendicular to the CCD propagation direction show the distribution of trapped charge at the silicon – dioxide interface. On the reference picture a high amount of charge is trapped under the gate at STI interface, whereas on the “wo STI” picture there is no charge trapped at STI interface. Therefore, the TCAD simulation shows a reduction of CTI due to a decrease of the amount of trapped charge at STI interface.

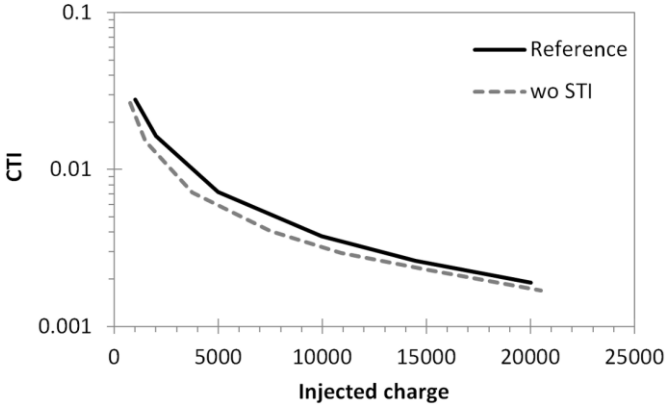


Fig. 5. 3D TCAD simulation of Charge Transfer Inefficiency vs injected charge of two different designs: reference and design without gate on STI.

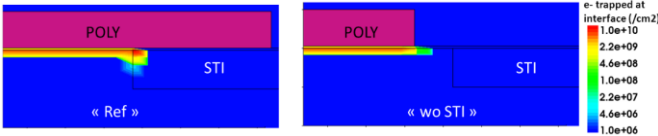


Fig. 6. 2D cross-sections perpendicular to the CCD direction showing electrons trapped at interface on the reference and on the “wo STI” designs.

Considering the positive TCAD simulation results, this

modification is implemented in the test chip.

### C. Variations on Pwell inclusion

In order to passivate STI edges, Pwell is drawn around the CCD channel with an inclusion of STI. By varying the Pwell inclusion of STI edges, we expect a modification of charge trapping, and consequently of CTI. In reality, the result should also depend on the technology used, as it is driven by the Pwell dopant distribution and by the STI oxide quality.

For this purpose, two Pwell inclusion variations are studied, one at 200 nm and another at 0 nm. The TCAD simulation was run with the same interface traps model for both STI and gate oxide, as we cannot calibrate them for both chosen technologies. In this way, the TCAD result is only depending on dopant distribution and not on the probably higher interface states of STI.

As can be seen in Fig. 7, reducing the Pwell inclusion at 0 nm leads to a small CTI reduction for more than 5000 injected electrons. This happens because the very thin Pwell layer between the STI and the CCD channel leads to a higher resulting potential, which gives a better electrostatic control of electrons. For a lower amount of injected electrons, the CTI is not reduced because the electrons transfer is mainly affected by interface traps rather than the improved potential in the vicinity of the CCD channel edges. Then, a Pwell inclusion of 200 nm induces a decrease of CTI (< 10%) in all injection range, due to a better passivation of STI edges which dramatically reduces contacts between electrons and STI. However, as said before, these observations have to be moderated and adapted, as it does not take into account the usual lower STI oxide quality. Indeed, if the interface traps densities are unbalanced at for example  $1 \times 10^9$  traps. $\text{cm}^{-2}$  for gate oxide and  $1 \times 10^{11}$  traps. $\text{cm}^{-2}$  for STI, CTI of the structure with 0 nm of Pwell inclusion strongly increases at the expense of the other two structures.

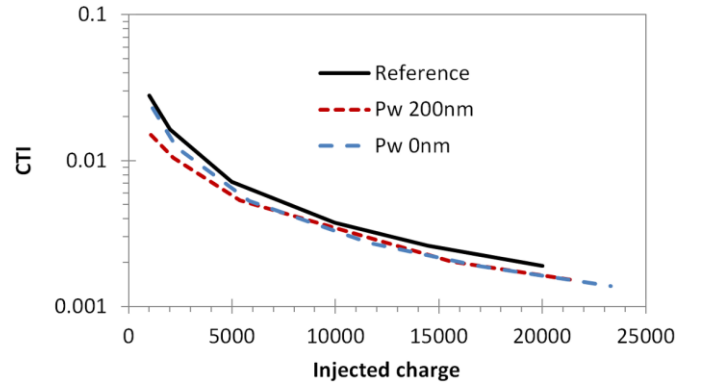


Fig. 7. 3D TCAD simulation of Charge Transfer Inefficiency vs injected charge of three different Pwell inclusion designs. The reference has a 100 nm Pwell inclusion.

These design variations are implemented in the test chips, and we expect different results depending on the technology used and on the Pwell inclusion.



### III. MEASUREMENTS ON TEST CHIPS

#### A. Experimental details

The various designs were implemented in two different test chips, manufactured in two different foundries. The first one, called “foundry A” is a leading Asian company providing a 180 nm imaging CMOS technology. The design rules fix the poly-silicon gap at 250 nm and no additional process option was taken. The second foundry, called “foundry B”, is a fab-less company providing an imaging CMOS technology with a poly-silicon gap fixed at 100 nm. In the same way, no additional process options were taken. The performances given by these two processes are not compared in this paper, as it is out of focus. Both test chips are compatible with surface channel transport (SCCD) as no buried channel was used. The two test chips were not designed and manufactured at the same time, and they do not have exactly the same design variations.

As in TCAD study, gates are 1  $\mu\text{m}$  long and 1  $\mu\text{m}$  wide, with a 100 nm Pwell inclusion for the reference design. For each design 2 structures were realized, one with 3 transfer gates and another one with 201 transfer gates. All CCD on CMOS devices are compatible with 3 phases CCD architectures. Electrons are injected by means of an injection drain and an injection gate, using the fill and spill method [13] [14]. Electrons are transferred to a floating diffusion node connected to a readout chain, similar to the ones used in CMOS imaging systems [1].

All measurements were performed at 22°C by means of a Cascade probe and a Pulse Instrument data generator. CTI was estimated using two methods, and averaged on 3 dies. The first one is the commonly used Extended Pixel Edge Response (EPER), which consists in measuring the amount of charge emerging in the first, second, etc. transfer following the charge transfer [15] [16]. This method gives a CTI based only on deferred electrons. The second one consists in a comparison between the transferred charge of a 3 gates structure and a 201 gates structure with the same design [11]. The method is called “Compared Pixel Response (CPR)”. Assuming that the CTI is constant over the entire CCD device, the CTI is calculated by means of the following formula:

$$CTI = \frac{\Delta V_{out\_3G} - \Delta V_{out\_201G}}{\Delta V_{out\_3G}} \frac{1}{(n_{201G} - n_{3G})} \quad (2)$$

where  $n_{3G}$  and  $n_{201G}$  are respectively the gate transfer number in the CCD test structure containing 3 transfer gates and 201 transfer gates,  $\Delta V_{out\_3G}$  is the voltage shift of the output node on the 3 gates structure, and  $\Delta V_{out\_201G}$  is the voltage shift of the output node on the 201 gates structure. The advantage of this method is to provide a CTI based on both deferred and lost charge. The mean dark current was also measured on all CCD on CMOS designs at 22°C by varying the storage time on one gate from 20  $\mu\text{s}$  to 180 ms.

In order to get representative results, the CTI is plotted vs the injected electrons. With the aim of obtaining the amount of injected electrons from the voltage shift of the output node, the

Charge to Voltage Factors (CVF) of the output nodes are estimated using their dimensions and the foundry capacitance model.

#### B. Measurements on test chips with gate design variations

The Fig. 8 is showing CTI measurements performed on the reference design (“ref”), the design with the conformed gates “form 2”, and the design with gates avoided on STI (“wo STI”), on chips processed in the foundry A. The Fig. 9 is showing CTI measurements obtained on the reference design (“ref”), and the design with gates avoid on STI (“wo STI”), on chips processed in the foundry B.

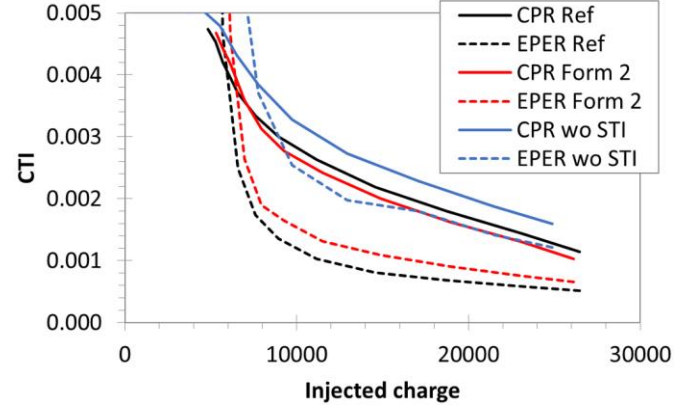


Fig. 8. Measurement of Charge Transfer Inefficiency vs injected charge of three different designs made in foundry A: reference, gate conformation “form 2”, and gate avoided on STI “wo STI”.

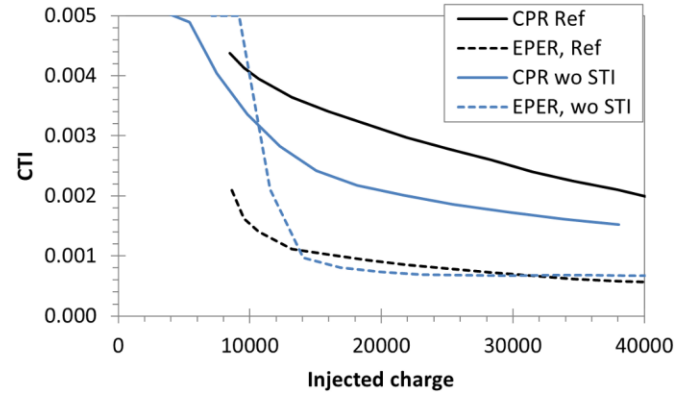


Fig. 9. Measurement of Charge Transfer Inefficiency vs injected charge of two different designs made in foundry B: reference, and gate avoided on STI “wo STI”.

The CTI measured on the reference designs give values comparable with other work [6] - [8], in the range of  $5.0 \times 10^{-4} < CTI (EPER, A) < 5.0 \times 10^{-3}$  and  $5.0 \times 10^{-4} < CTI (EPER, B) < 2.0 \times 10^{-3}$ . As expected, the CTI measured by EPER is lower compared to the CTI measured by CPR, because CTI measured by EPER takes into account only deferred charge and miss lost charge. Therefore, the CTI measured by CPR is in the range of  $1.1 \times 10^{-3} < CTI (CPR, A) < 5.0 \times 10^{-3}$  and  $1.8 \times 10^{-3} < CTI (CPR, B) < 4.4 \times 10^{-3}$ . As usually observed [15] - [17], CTI strongly increases when injected electrons are getting smaller due to the presence of interface states at the

silicon – oxide interface. Indeed, smaller amount of electrons have a lower charge density, and therefore the smaller electrons packets interact with more traps per electron of signal, leading to an increase of the CTI.

The CTI of the device with gates conformed “Form 2” is similar to the reference sample (foundry A). This disappointing result can be attributed to the fact that we had to violate lot of design rules when we drew this pattern. Indeed, the original gate shape requires to draw slanted lines and to cross diffusion regions without respecting the minimum clearance distance. It might be possible that the gate oxide thickness or its quality is affected by the non-compliance of these design rules which lead to the realization of the gate and gate oxide process in non-optimized and non-recommended conditions. Thus, electrons transfer is affected by the presence of defects or potential barrier due to gate oxide modifications.

If we look now at the design with gates avoided on STI (“wo STI”), we see a slight increase of the CTI with the foundry A, in contrary to the TCAD prediction. However, in the same way as for the “form 2” sample, we had to violate some design rules. Indeed, the minimum clearance distance between poly and diffusion area cannot be respected in this structure and poly-silicon contacts on diffusion were drawn whereas it is not allowed. One can suppose that this affects the gate oxide or the gate quality. Consequently, electrons transfer is affected by the presence of defects or by potential barrier as with the gate conformed “form 2”. On the sample made in the foundry B, we see a reduction of the CTI measured by CPR of about 15%, meaning that less charge are lost during the transfer, in agreement with the TCAD. This design modification reduces the CTI only with the foundry B, probably because design rules of the foundry B allow the poly-silicon contact on diffusion and enforce less restrictive clearance distance between poly and diffusion area. The gates and gate oxide are therefore realized in optimized conditions and electrons transfer is only affected by the gate conformation. To conclude, this kind of design modification can reduce the CTI, but it mainly depends on the technology used.

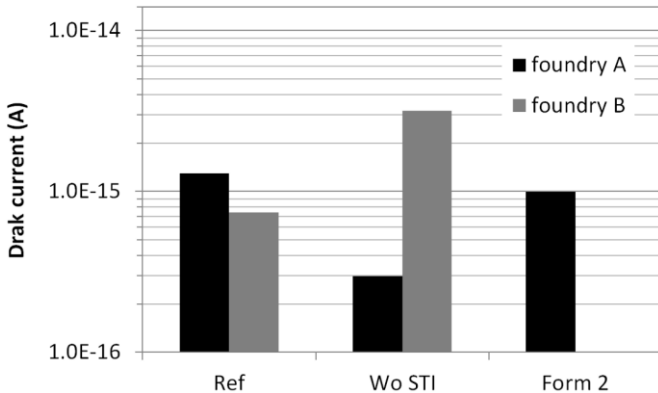


Fig. 10. Measurement of dark current for different designs made in foundry A and B: reference, gate avoided on STI “wo STI”, and gate conformed “form 2”.

Dark current measurements are shown in the Fig. 10. The

dark current seems to be not sensitive to the design modification “Form 2”. However, with the gates avoided on STI, the dark current is divided by 3 or multiplied by 2 depending on the technology used. Therefore, we cannot conclude on the dark current variation with the gate avoided on STI.

To conclude, the gate design variations do not lead to obvious CTI reduction. Indeed, the processed chips did not give the expected results like the ones shown by TCAD simulations, probably because such variations require to violate a lot of design rules, which can degrade the region where charge are moving.

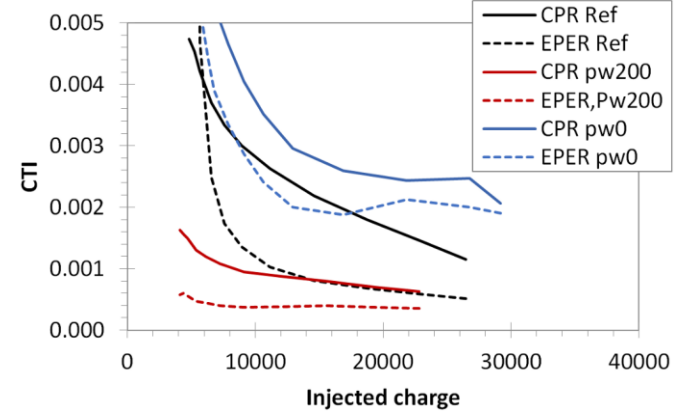


Fig. 11. Measurement of Charge Transfer Inefficiency vs injected charge of three different designs made in foundry A: reference (100 nm inclusion), 200 nm Pwell inclusion and 0 nm Pwell inclusion.

### C. Measurements on test chips with Pwell inclusion variations

Measurement performed on CCD on CMOS devices with various Pwell inclusions are shown in Fig 11 (foundry A) and in Fig. 12 (foundry B).

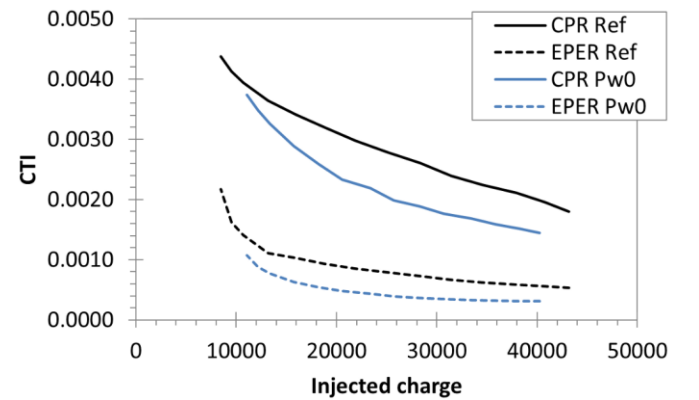


Fig. 12. Measurement of Charge Transfer Inefficiency vs injected charge of two different designs made in foundry B: reference (100 nm inclusion) and 0 nm Pwell inclusion.

A Pwell inclusion of 200 nm gives a very nice CTI reduction with technology A, measured by CPR and by EPER. Indeed, the CTI is decreased until 60% and is in the range of  $6.3 \times 10^{-4} < \text{CTI (by CPR)} < 1.6 \times 10^{-3}$  and  $3.6 \times 10^{-4} < \text{CTI (by EPER)} < 6.0 \times 10^{-4}$ . As it was found previously that STI edges

in foundry A have much more interface states than gate oxide, increasing the Pwell inclusion over STI edges lead to a strong reduction of electrons trapping.

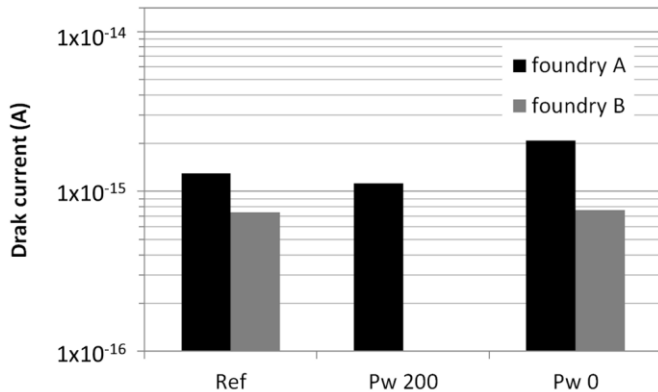


Fig. 13. Measurement of dark current for different designs made in foundry A and B: reference, Pwell inclusion of 200 nm over STI (Pw 200), and Pwell inclusion of 0 nm over STI (Pw 0).

Dark current was evaluated on these CCD test structures and results are displayed in the Fig. 13. The technology A has lower STI oxide quality compare to gate oxide and dark current evolves in agreement with this observation: a 0 nm Pwell inclusion increases the dark current and a 200 nm Pwell inclusion decreases it. The results obtained on technology B are less sensitive to Pwell inclusion and only a small dark current increase is visible with a Pwell inclusion of 0 nm.

The influence of Pwell inclusion is mainly dependent on the technology used. Therefore, when STI oxide has a lower interface quality than gate oxide, which is usually the case, a higher Pwell inclusion leads to a CTI reduction and potentially to a dark current reduction.

In a future work higher values of Pwell inclusion will be studied as well as the use of a higher doped implantation instead of Pwell on the vicinity of the CCD channel. The ambition is to improve again the STI passivation and to decrease the CTI.

#### IV. CONCLUSION

The design impact study on charge transfer inefficiency was conducted by means of 3D TCAD simulations and measurements performed on 2 test chips manufactured on 2 different foundries. TCAD simulations show a reduction of CTI using a modified “V” shape of the gate, which is not verified on the measurement performed on one chip, probably because of the design rules we had to violate. In the other hand, TCAD suggests a reduction of trapped charge during transfer when the poly-silicon gate is only drawn over diffusion area and not on STI. Actually, measurements indicate a CTI reduction of about 15% only with the technology allowing this kind of design exception. Finally, a variation on Pwell inclusion on STI edges was realized. TCAD simulations with an identical trap model at gate oxide and STI oxide interfaces show a small reduction of CTI (< 10%) when the Pwell inclusion is chosen at 200 nm. This was

verified by measurement, the CTI measured on the chip with a worse STI oxide quality compared to gate oxide shows a strong CTI reduction of 60%. To conclude, TCAD simulations are in a good agreement with measurement trend, but a specific trap model calibration has to be done for each technology in order to improve the predictability of the simulator. Therefore, if the technology used provides a lower STI interface quality than the gate oxide interface, CTI can be reduced by increasing the Pwell inclusion on STI edges at the expense of the foundry recommendation.

#### REFERENCES

- [1] A.J.P. Theuvsen, “CMOS image sensors: State-of-the-art,” *Solid St. Electron.*, vol. 52, pp. 1401-1406, May 2008.
- [2] P. Lee, R. Gee, M. Guidash, T. Lee, and E. R. Fossum, “An active pixel sensor fabricated using CMOS/CCD process technology,” in *Proc. IEEE Workshop on CCDs and Advanced Image Sensors*, pp. 115-119, Apr. 20-22, 1995.
- [3] G. Lepage, J. Bogaerts, G. Meynants, “Time Delay Integration in CMOS image sensors,” *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2524-2533, Nov. 2009.
- [4] N. Mutoh, S. Kawai, T. Yamada, Y. Kawakami, T. Nakano, K. Orihara, and N. Teranishi, “Driving Voltage Reduction of Shift Registers in IT-CCD Image Sensors,” in *Proc. IEEE Workshop on CCDs and Advanced Image Sensors*, pp R17-1 – R17-4, Jun. 5-7, 1997.
- [5] M. J. Howes, D. V. Morgan, “*Charge-coupled Devices and System*”, Wiley, 1979.
- [6] J. Borg and J. Johansson, “Evaluation of a Surface-Channel CCD Manufactured in a Pinned Active-Pixel-Sensor CMOS Process,” *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2660-2664, Aug. 2011.
- [7] K. Fife, Abbas El Gamal and H.-S. Philip Wong, “A 0.5μm Pixel Frame-Transfer CCD Image Sensor in 110nm CMOS,” in *Proc. IEEE Electron Devices Meeting*, pp. 1003-1006, Dec. 10-12, 2007.
- [8] F. Mayer, H. Bugnet, S. Pesenti, C. Guicherd, B. Gili, R. Bell, B. De Monte, and T. Ligozat, “First Measurements of True Charge Transfer TDI (Time Delay Integration) Using a Standard CMOS Technology”, *International Conference on Space Optics*, Oct. 9-12, 2012.
- [9] R. Hoople, “Characteristics of Submicrometer Gaps in Buried-Channel CCD Structures,” *IEEE Trans. Electron Devices*, vol. 38, no. 5, pp. 1175-1181, May 1991.
- [10] T. Lee, T. J. Tredwell, B. C. Burkey, T. M. Kelly, R. P. Khosla, D. L. Losee, R. L. Nielsen, and W. C. McColgin, “A 360000 Pixel Charge-Coupled Color-Image Sensor for Imaging Photographic Negative,” *IEEE Trans. Electron Devices*, vol. ED-32, no. 8, pp. 1439-1445, Aug. 1985.
- [11] O. Marcelot, M. Estribeau, V. Goiffon, P. Martin-gonthier, F. Corbière, R. Molina, S. Rolando, and P. Magnan, “Study of CCD Transport on CMOS Imaging Technology: Comparison Between SCCD and BCCD, and Ramp Effect on the CTI”, *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 844-849, Mar. 2014.
- [12] V. Goiffon, C. Virmondois, P. Magnan, S. Girard, and P. Paillet, “Analysis of Total Dose-Induced Dark Current in CMOS Image Sensors From Interface State and Trapped Charge Density Measurements”, *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3087-3094, Dec. 2010.
- [13] G. Prigozhin, and B. Burke, “CCD Charge Injection Structure at Very Small Signal Levels,” *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2111-2120, Aug. 2008.
- [14] M.F. Tompsett, “Surface Potential Equilibration Method of Setting Charge in Charge-Coupled Devices,” *IEEE Trans. Electron Devices*, vol. ED-22, no. 6, pp. 305-309, Jun. 1975.
- [15] R.W. Brodersen, D.D. Buss, and A.F. Tasch, “Experimental Characterization of Transfer Efficiency in Charge-Coupled Devices,” *IEEE Trans. Electron Devices*, vol. ED-22, no. 2, pp. 40-46, Feb. 1975.
- [16] A. Waczynski, E. J. Polidan, P. W. Marshall, R. A. Reed, S. D. Johnson, R. J. Hill, G. S. Delo, E. J. Wassell, and E. S. Cheng, “A Comparison of Charge Transfer Efficiency Measurement Techniques on Proton Damaged n-Channel CCDs for the Hubble Space Telescope Wide-Field Camera 3,” *IEEE Trans. Nuc. Sci.*, vol. 48, no. 6, pp. 1807-1814, Dec. 2001.

- [17] J. R. Janesick ; G. B. Soli ; T. S. Elliott and S. A. Collins, "Effects of proton damage on charge-coupled devices", in Proc. SPIE 1447 Charge-Coupled Devices and Solid State Optical Sensors II, vol. 1447, pp 87-108, Jul. 1, 1991
- [18] T. Hardy, R. Murowinski, and M. J. Deen, "Charge Transfer Efficiency in Proton Damaged CCD's", *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 154–163, Apr. 1998